CLAIMS

I claim:

1. A method for issuing instructions in a multithreaded computer processor, the method comprising the steps of:

receiving sets of computer instructions in an instruction issue logic, wherein each set of instructions comprises one instruction from each of a plurality of independent instruction threads;

predicting a stage, within a multi-stage instruction pipeline of the computer processor, where results of each instruction will be available;

identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

determining a confidence factor for each received instruction that indicates a probability that the instruction will complete all stages of the pipeline without causing a stall; and,

issuing, from the instruction issue logic, instructions with confidence factors above a predetermined threshold.

2. The method of claim 1, further comprising the steps of:

storing the predicted pipeline stage for each instruction; and,

dynamically updating the stored predicted pipeline stage for each instruction based on a current contents of the pipeline.

3. The method of claim 2, wherein the confidence factor for an instruction is determined based upon a current location and the predicted stage of the prerequisite instruction.

4. The method of claim 3, further comprising the step of:

dynamically recalculating the confidence factor for each instruction based on the current contents of the pipeline.

5. The method of claim 2, further comprising the step of:

identifying as dependent instructions those received instructions that have a conflict over a shared resource within a computer system in which the computer processor operates.

6. The method of claim 5, wherein the confidence factor for a dependent instruction is determined based upon the current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

7. The method of claim 6, further comprising the step of:

dynamically recalculating the confidence factor for each instruction based on the current contents of the pipeline and a current status of any shared resources.

8. A method for issuing instructions in a single threaded computer processor, the method comprising:

receiving sets of computer instructions in an instruction issue logic, wherein each set of instructions comprises multiple instructions from a single instruction thread;

predicting a stage, within a multi-stage instruction pipeline of the computer processor, where results of each instruction will be available;

identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

determining a confidence factor for each received instruction which indicates a probability that the instruction will complete all stages of the pipeline without causing a stall; and,

issuing, from the instruction issue logic, instructions whose confidence factor is above a predetermined threshold.

9. The method of claim 8, further comprising the steps of:

storing the predicted pipeline stage for each instruction; and,

dynamically updating the stored predicted pipeline stage for each instruction based on a current contents of the pipeline.

10. The method of claim 9, wherein the confidence factor for an instruction is determined based upon a current location and the predicted stage of the prerequisite instruction.

11. The method of claim 10, further comprising the step of:

dynamically recalculating the confidence factor for each instruction based on the current contents of the pipeline.

12. The method of claim 9, further comprising the step of:

identifying as dependent instructions those received instructions that require an operand from a memory of a computer system in which the computer processor operates.

13. The method of claim 12, wherein the confidence factor for a dependent instruction is determined based upon a current location and the predicted stage of any prerequisite instruction and upon a probability that any required operand will be found in a cache memory of the processor.

14. The method of claim 13, further comprising the step of:

dynamically recalculating the confidence factor for each instruction based on the current contents of the pipeline and a current contents of the processor cache memory.

15. The method of claim 1, wherein one or more instruction(s) is(are) issued from the instruction issue logic at each clock cycle.

16. A simultaneous multithreaded computer processor with speculative instruction issue that increases throughput, the computer processor comprising:

multiple independent input buffers, wherein one set of buffers is provided for each of a plurality of independent threads of instructions;

instruction issue logic that is connected to the independent input buffers, wherein the instruction issue logic:

receives instructions from each of the threads of instructions;

predicts a stage, within a multi-stage pipeline of the processor, in which a result from each instruction will be available;

identifies as dependent instructions those received instructions that require a result from a prerequisite instruction;

determines a confidence factor for each instruction that indicates a probability that the instruction will complete all stages of the multi-stage pipeline without causing a stall; and,

issues instructions with confidence factors above a predetermined threshold;

and, wherein a first stage of the multi-stage pipeline is connected to an output buffer of the instruction issue logic.

17. The computer processor of claim 16, wherein the instruction issue logic stores the predicted pipeline stage for each instruction and, dynamically updates the stored predicted pipeline stage for each instruction based on a current contents of the pipeline.

18. The computer processor of claim 16, wherein the confidence factor for an instruction is determined based upon a current location and the predicted stage of the prerequisite instruction.

19. The computer processor of claim 17, wherein the instruction issue logic dynamically recalculates the confidence factor for each instruction based on the current contents of the pipeline.

20. The computer processor of claim 16, wherein one or more instruction(s) is(are) issued from the instruction issue logic every clock cycle.

21. The computer processor of claim 16, wherein the instruction issue logic further identifies as dependent instructions those received instructions that have a conflict over a shared resource within a computer system in which the computer processor operates.

22. The computer processor of claim 21, wherein the confidence factor for a dependent instruction is determined based upon a current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

23. The computer processor of claims 22, wherein the instruction issue logic dynamically recalculates the confidence factor for each instruction based on a current contents of the pipeline and a current status of any shared resources.

24. A single threaded computer processor with speculative instruction issue that increases throughput, the computer processor comprising:

multiple input buffers for receiving instructions from a thread of instructions;

instruction issue logic that is connected to the input buffers, wherein the instruction issue logic:

receives instructions from the input buffers;

predicts a stage, within a multi-stage pipeline of the processor, in which a result from each instruction will be available;

identifies as dependent instructions those received instructions that require a result of a prerequisite instruction;

determines a confidence factor for each instruction that indicates a probability that the instruction will complete all stages of the pipeline without causing a stall; and,

issues instructions with confidence factors above a predetermined

threshold;
and, wherein a first stage of the multi-stage pipeline is connected to an output buffer of the instruction issue logic.

25. The computer processor of claim 24, wherein the instruction issue logic stores the predicted pipeline stage for each instruction and, dynamically updates the stored predicted pipeline stage for each instruction based on a current contents of the pipeline.

26. The computer processor of claim 24, wherein the confidence factor for an instruction is determined based upon a current location and the predicted stage of the prerequisite instruction.

27. The computer processor of claim 25, wherein the instruction issue logic dynamically recalculates the confidence factor for each instruction based on the current contents of the pipeline.

28. The computer processor of claim 24, wherein the instruction issue logic further identifies as dependent instructions those received instructions that have a conflict over a shared resource within a computer system in which the computer processor operates.

29. The computer processor of claim 28, wherein the confidence factor for a dependent instruction is determined based upon a current location and the predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

30. The computer processor of claims 29, wherein the instruction issue logic dynamically recalculates the confidence factor for each instruction based on a current contents of the pipeline and a current status of any shared resources.